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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,416	10/23/2003	Anthony Gus Aipperspach	AUS920030577US1	8492

50170 7590 10/20/2006

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EXAMINER	
ALMO, KHAREEM E	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,416	AIPPERSPACH ET AL.	
	Examiner	Art Unit	
	Khareem E. Almo	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19,22 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,22 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-19 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sher (US 2001/0011913).

With respect to claim 1, figure 2 of Sher discloses a pulse width limiting circuit, comprising: a clock signal correction block (3, 5,7, 9 and 27) configured to receive a conditioned clock signal (XCLK) and generate a corrected clock output signal (at node D), wherein the clock signal comprises a train of clock pulses, each of which has a rising clock edge, a falling clock edge and a variable width; a block delay module (21, 23 and 25) coupled to the clock signal correction block configured to accept an unconditioned clock signal (CLKY) and introduce a specified pulse width delay to thereby generate the conditioned clock signal, wherein the block delay module comprises a plurality of delay sub-blocks of fixed delay; and a high low clock pulse shuttle circuit (elements of 11) coupled to the clock signal correction block, configured to accept the conditioned clock signal output (at node D), but fails to disclose the high low clock pulse shuttle comprising a first field effect transistor (FET) coupled to the

correction block and a second FET coupled to a conditioned clock signal interconnect and wherein individual delay sub-blocks of the plurality of delay sublocks of the block delay module are disconnected and reset based on the unconditioned clock signal. "DIGITALINTEGRATED CIRCUITS –A Design Perspective", Jan M. Rabaey, Prentice Hall (1996) Chapter 4, page 193 teaches the internal elements of a two input NAND gate using CMOS technology. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use combinational FETs to make the NAND gate of Sher for the well known purpose of minimizing power consumption.

With respect to claim 2, the resulting combination above produces a circuit wherein the unconditioned clock signal is input to the drain of a p-type FET in the high low clock pulse shuttle (p-type FET's of 11).

With respect to claim 3, the resulting combination above produces a circuit wherein the system comprises a leak detector unit (3) coupled to the clock signal correction block, wherein the clock signal correction block is employed to transmit the conditioned clock signal to the high low clock pulse shuttle (p-type FETs of 11).

With respect to claim 4, the resulting combination above produces a circuit wherein the high low clock pulse shuttle (p-type FETs of 11) is coupled to an interconnect (wire between 11 and 13), wherein the interconnect is employed to convey the unconditioned clock signal.

With respect to claim 5, the resulting combination above produces a circuit further comprising a node (going into 21) to transmit a clock pulse of the unconditioned clock signal between stages of a delay sub-block (21, 23 and 25).

With respect to claim 6, the resulting combination above produces a circuit, further comprising a node (at C) to transmit a clock signal between a last delay sub-block (21, 23, and 25) of the plurality of delay sub-blocks and the clock signal correction block (3, 5, 7, 9 and 27).

With respect to claim 7, the resulting combination above produces a circuit, further comprising a node (at node Y) to transmit the conditioned clock signal between the clock signal correction block (3, 5, 7, 9 and 27), the high low clock pulse shuttle circuit (p-type FETs of 11) and a clock pulse inverter (13).

With respect to claim 8, the resulting combination above produces a circuit further comprising a leak detector (3) calculating a voltage potential between two digital devices.

With respect to claim 9, the resulting combination above produces a circuit wherein an uncorrected clock pulse bypasses the clock signal (via n-type gates of 11 and wire between 11 and 13) correction block (3, 5, 7, 9 and 27) and the high low clock pulse shuttle circuit (p-type FETs of 11) for delivery through the clock pulse inverter (13).

With respect to claim 20, the resulting combination above produces a circuit comprising: a means for determining undesirable clock pulse width (3); a means (21, 23 and 25) for forwarding undesired clock pulses to a correction block (3, 5, 7, 9 and 27); a means (n-type FETs of element 11 and wire between 11 and 13), for desired clock pulses to bypass the pulse width correction and go directly to the device output; and a means (p-type FETs of 11) for incrementing a sequential delay for cascading a series of

delay sub-blocks (21, 23 and 25).

With respect to claim 21, the resulting combination above produces a circuit comprising: a means for determining undesirable clock pulse width (3); a means (21, 23 and 25) for forwarding undesired clock pulses to a correction block (5, 7, 9 and 27); a means (n-type FETs of element 11 and wire between 11 and 13) for bypassing the correction block (3, 5, 7, 9 and 27) sending desired clock pulses directly to the device output; and a means (p-type FETs of 11) for incrementing a sequential delay for cascading a series of delay sub-blocks (21, 23 and 25).

With respect to claim 23, this claim is rejected for similar reasons as above.

2. The indicated allowability of claims 10-19 are withdrawn in view of the newly discovered reference(s) to Sher. Rejections based on the newly cited reference(s) follow.

With respect to claims 10-19 and 22, the methods are deemed to read on the combination of the circuits produced above.

Response to Arguments

3. Applicant's arguments filed 6/29/2006 have been fully considered but they are not persuasive.

With respect to the examiner's view on the allowable claims this has been withdrawn due to a clearer understanding of the claimed invention. In the original application it was unclear as to how the disconnection and reconnection was achieved.

It has since become clear this disconnection and reconnection is not achieved by an open circuit switch but by bypassing a switch. The circuit is not broken and thus the prior art of record can read on this circuit.

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khareem E. Almo whose telephone number is (571) 272-5524. The examiner can normally be reached on Mon-Fri (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KEA
10/16/2006

Quan Tra
Primary Examiner